(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 049 247 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
02.11.2000 Bulletin 2000/44

(51) Int Cl.7: H03F 3/217

(21) Application number: 99830247.5

(22) Date of filing: 27.04.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: STMicroelectronics S.r.l.
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- Masini, Marco
20162 Milano (IT)
- Franchini, Luigi
47037 Rimini (IT)
- Labbe, Eric
20010 Cornaredo (IT)

(74) Representative: Pellegri, Alberto et al
c/o Società Italiana Brevetti S.p.A.,
Piazza Repubblica 5
21100 Varese (IT)

(54) Class-D amplifier with enhanced bandwidth

(57) A class-D amplifier comprising an input integrating stage *(Op-Amp, R1, C)*, a modulating stage (PWM) of the integrated input signal output by said integrating stage, using as a carrier an alternate waveform (*Vtr*) of a frequency (*fsw*), sufficiently higher than the frequency band of the analog input signal, outputting a digital signal switching between a positive voltage (*+Vcc*) and a negative voltage (*-Vcc*), and whose average value (*Vo*) represents an amplified replica of the input analog signal, an output power stage (BUFFER), producing an output digital signal (*Vout*), a feedback line constituted by a resistor (*R2*) connected between the output of said output power stage (BUFFER) and an input node of an operational amplifier (*Op-Amp*) constituting said integrating stage, and a low pass filter reconstructing an output analog signal (*Vo*), further comprises a delay stage (DELAY *Td*), functionally coupled in the direct path of propagation of said digital signal from the output of said PWM stage to an input of said output power stage (BUFFER), delaying said digital signal by a delay (*Td*) whose value is defined in function of a desired broadening of the bandwidth and in consideration of the corresponding restriction of the range of variation of the duty-cycle of the output digital signal.

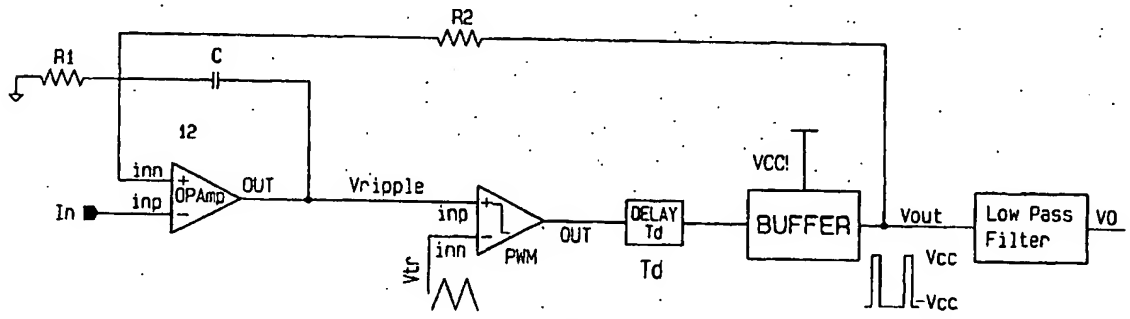

FIG.6

EP 1 049 247 A1

Description

FIELD OF THE INVENTION

[0001] The present invention relates to Class-D PWM amplifiers.

STATE OF THE ART

[0002] Fig. 1 shows the typical scheme of a Class-D amplifier.

[0003] This type of amplifier is a well-known PWM system (re: K. Nielsen, "Review and Comparison of PWM methods for analog and digital input switching power amplifiers" AES 22-25/3/97).

[0004] The operation of the amplifier is depicted in Fig. 2.

[0005] The input signal (*Vin*) is compared with a waveform, most often triangular (*Vtr*) having a relatively high frequency *fsw* much higher than the frequency band limit of the amplifier.

[0006] The output (*Vout*) is a PWM (Pulse Width Modulated) signal switching between a positive voltage (*Vcc*) and a negative voltage (*-Vcc*).

[0007] The average value (*Vo*) of the output digital signal represents an amplified replica of the analog input signal and may be easily calculated with the following equations:

$$Vo = G \cdot Vin \tag{1}$$

$$G = \frac{Vcc}{Vtr} \tag{2}$$

where *Vtr* is the peak value of the reference (triangular) wave and *G* is the voltage gain of the amplifier.

[0008] The relationship between *Vo* and *Vin* is thereby theoretically linear. In practice though this is not true because the non-idealities of the triangular wave and of the output buffer stage may produce an unacceptable amount of distortion on the output signal.

[0009] Therefore, a feedback loop capable of compensating the non-idealities of the system is a must.

[0010] A typical feedback circuit is shown in Fig. 3

[0011] Given that the average charge of the integrating capacitor C must be null during a switching period (*Tsw=1/fsw*), it may be assumed that the average current on the feedback resistor *R2* during a switching period is equal to the current on the input resistor *R1* and therefore:

$$Vo = G_c \cdot Vin \tag{3}$$

$$G_c = 1 + \frac{R_2}{R_1} \tag{4}$$

where *Gc* is the closed loop gain of the system.

[0012] The. open loop gain *Gloop* of the system may be easily calculated by analyzing the scheme of Fig. 4, wherein a linearized system is considered with the *Vin* node short-circuited to ground and the PWM stage substituted with a linear block with a gain *Vcc/Vtr* (re: equation 2).

[0013] The input resistor *R1* has been neglected because, at the frequencies of interest, the negative input of the integrator represents a virtual ground (because the integrating capacitor *C* represents an extremely low impedance) and therefore there is not any significative voltage drop on the input resistor *R1*.

[0014] The open loop gain Gloop and the unity gain frequency are thus respectively defined by:

$$G_l(s) = \frac{Vcc}{Vtr} \cdot \frac{1}{s \cdot R2 \cdot C} \tag{5}$$

$$f_o = \frac{1}{2\pi} \cdot \frac{Vcc}{Vtr} \cdot \frac{1}{R2 \cdot C} \tag{6}$$

[0015] This system has a stability limit that limits the system's bandwidth.

[0016] This limit may be calculated (by referring to Fig. 3) by considering that for a correct functioning of the system, the slope of the ripple signal (*Vr*) must be lower than the slope of the triangular wave (*Vtr*).

[0017] If this condition is not met, the system may produce repeated output switchings at intervals equal to the delay of the chain delay defined by the PWM stage and by the output buffer stage.

[0018] Correct and critical functioning conditions are schematically depicted in the diagrams of Fig. 5.

[0019] By converting this concept into formulas:

$$p_1 = 4 \cdot Vtr \cdot fsw \qquad \text{(slope of triangular waveform)} \tag{7}$$

$$p_2 = \frac{1}{C} \cdot \left(\pm \frac{Vcc}{R2} - \frac{Vin}{R1} \right) \qquad \text{(slope of the ripple)} \tag{8}$$

[0020] To obtain the limit condition the maximum slope of the ripple signal should be considered, in other words the maximum input signal Vin_{max}.

[0021] From equations (3), (4):

$$Vin_{max} = \frac{Vcc}{Gt} \tag{9}$$

[0022] Therefore, the maximum *p2* value is given by:

$$p_{2,max} = \frac{1}{C} \cdot \left(\frac{Vcc}{R2} + \frac{Vcc}{R1 \cdot Gt} \right) = \frac{Vcc}{C} \cdot \left(\frac{1}{R2} + \frac{1}{R1 + R2} \right) = \frac{Vcc}{R2 \cdot C} \cdot \left(1 + \frac{R2}{R1 + R2} \right) \tag{10}$$

[0023] Therefore, the limit condition is:

$$p_{2,max} = \frac{Vcc}{R2 \cdot C} \cdot \left(1 + \frac{R2}{R1 + R2} \right) \leq 4 \cdot Vtr \cdot fsw = p_1 \tag{11}$$

[0024] Considering equation (6), this condition may be rewritten as:

$$f_0 \leq \frac{2}{\pi} \cdot \frac{1}{\left(1 + \frac{R2}{R1 + R2} \right)} \cdot fsw \tag{12}$$

which represents a bandwidth limit. It should be noticed that for a *Ggain>10* (that is for *R2/R1>10*), equation (12) may simplified into the following equation:

$$f_0 < \frac{fsw}{\pi} \tag{13}$$

OBJECT AND SUMMARY OF THE INVENTION

[0025] Confronted with these limitations and drawbacks of known amplifiers, a manner has now been found to overcome this limiting critical condition and allow for an extended bandwidth at the expense of a negligible reduction of the

range of variation of the duty-cycle of the digital output signal.

[0026] The amplifier of the present invention functions even when the slope of the triangular wave is lower than the slope of the ripple of the input signal without causing spurious repetitive switchings of the output signal.

[0027] This important result is obtained by introducing a certain delay on the direct signal path, downstream of the PWM output stage, and in any case before the output node from which the feedback signal is derived for compensating the nonidealities of the system.

[0028] The invention is defined in claim 1.

[0029] The various aspects and effects of the invention are described with more details in the following description of an embodiment and with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030]

Figure 1 shows the basic scheme of a class-D amplifier;
Figure 2 shows the characteristic waveforms of a PWM amplifier;
Figure 3 is a functional block diagram of a class-D amplifier of a known type;
Figure 4 is a simplified open loop analysis model of the amplifier of Fig. 3;
Figure 5 shows diagrams illustrative of the stability limit of a known amplifier;
Figure 6 is a functional block diagram of a class-D amplifier according to the present invention;
Figure 7 is a diagram illustrating the effect of the delay introduced according to the present invention;
Figure 8 is a scheme of the functioning conditions of the amplifier of the invention;
Figure 9 shows the maximum allowable ratio between the slope of the ripple and the slope of the triangular waveform without causing instability problems;
Figure 10 shows the characteristic of bandwidth increment in function depending of the introduced delay;
Figure 11 shows the characteristic of bandwidth increment in function of the maximum duty-cycle;
Figure 12 shows a possible embodiment of the delay circuit;
Figure 13 shows the waveforms of the delay circuit for a duty-cycle of 50%;
Figure 14 shows the waveforms for a duty-cycle close to its maximum limit.

GENERAL DESCRIPTION OF THE INVENTION

[0031] The functional diagram of a class-D amplifier according to the present invention is shown in Fig. 6. By way of comparison with the diagram of Fig. 3 of an amplifier realized according to know techniques, the only element that is introduced is the block DELAY *Td,* coupled in the direct signal path, in cascade to the output of the comparator PWM and, preferably, before the output power stage BUFFER.

[0032] The functioning with and without the introduction of the delay *Td* is shown in Fig. 7. It may be immediately concluded that the introduction of the delay *Td* permits the system to function satisfactorily even with a larger slope of the ripple (p2b) than the slope of the triangular wave, without causing spurious switchings of the output.

[0033] For an accurate calculation of the improvement of the bandwidth limit when using the delay block of the invention, it should be considered that the introduction of the delay changes the PWM stage gain (the larger is the introduced delay the lower is the gain). Moreover, differently from what occurs in a known system, the most critical condition for the stability of a system with a delay block, according to the present invention, coincides with that of an average duty-cycle and not with that of maximum or minimum duty-cycle as it was the case in a known system.

Bandwidth calculation

[0034] The starting hypothesis is the following.

[0035] The PWM modulator may be considered, for bandwidth calculation, as a linear block with a voltage gain given by the ratio between the average of the output signal and the average of the ripple signal.

[0036] The calculation entails three steps:

1) expressing the PWM modulator gain as a function of the delay;
2) defining the stability conditions;
3) calculating the maximum bandwidth allowed.

[0037] Fig. 8 indicates the parameter notation adopted for the analysis and calculation.

1) Gain of the PWM modulator

[0038] The following equations among the parameters involved area readily verified:

$$p1 = p \cdot (1 - d) \qquad p2 = pd \qquad pt = 4\,Vtr \cdot fsw \qquad Toff = (1 - d)/fsw \qquad p = 2Vcc/\tau$$

where d is the duty-cycle, $2*p$ is the slope of the ripple for $d=0.5$, pt is the slope of the triangular wave, Vtr is the peak voltage of the triangular wave, fsw is the switching frequency and τ is the time constant of the system ($\tau=R2 \cdot C$, re: Fig. 6).

[0039] By using these equations, it is useful to express the voltages $V1$ and $V2$ of Fig. 8 with geometrical considerations and thereby the average voltage of the ripple signal.

[0040] The result is that the voltage gain of the PWM modular, as defined in the starting hypothesis, is given by:

$$G_{PWM} = G_0 \cdot \frac{1}{1+G_0 \cdot (Td/\tau)} \tag{14}$$

where $G0$ is the gain in absence of delay ($G0=Vcc/Vtr$) and Td is the delay. Therefore, the delay reduces the gain of the PWM modulation stage.

2) Stability conditions

[0041] It is useful to introduce a new parameter defined by:

$$\alpha = \frac{p}{p_t}$$

[0042] Therefore, $2*\alpha$ represents the ratio of the calculated slope of the ripple with $d=0.5$ and the slope of the triangular wave.

[0043] Thus, the problem is to establish the maximum admissible value of the parameter a without generating stability problems.

[0044] With reference to Fig. 8, the stability condition is given of course by the equality $V2=Vtr$.

[0045] Upon imposing this condition, in order to guarantee the stability throughout the whole range of variation of the duty-cycle field, the ratio α must be less than the limit value $\alpha max.$, whose value is shown in the diagram of Fig. 8.

[0046] For example, with a delay of 200ns, a system with a α factor of about 1.6 may be implemented without any stability problems.

3) Maximum allowed bandwidth

[0047] From the starting hypothesis on the PWM modulator gain, it follows that the bandwidth of the system (that is the unity open loop gain frequency) is given by:

$$f_0 = \frac{G_{PWM}}{2\pi \cdot \tau} \tag{15}$$

[0048] Using the equation (14), the equation (15) may be rewritten as a function of the α parameter:

$$f_0 = \frac{fsw}{\pi} \cdot \frac{\alpha}{1+(2 \cdot Td \cdot fsw) \cdot \alpha} \tag{16}$$

[0049] Since fsw/π represents the maximum bandwidth with $Td=0$, an expression of the bandwidth improvement (β factor) due to the delay introduced may be expressed as:

$$\beta = \frac{f_0 \cdot \pi}{fsw} = \frac{\alpha}{1+(2 \cdot Td \cdot fsw) \cdot \alpha} \tag{17}$$

[0050] By introducing the equation (17) the maximum value of the α factor for a certain delay *Td* (re: Fig. 9), the maximum bandwidth increment of the bandwidth ($\beta max.$) for the considered delay *Td* may be calculated.

[0051] Fig. 10 shows the bandwidth improvement factor β as a function of the delay (for a switching frequency *fsw=200KHz*).

[0052] For example, with a delay of 300ns the improvement is of about 60%.

[0053] In any case, the maximum usable delay is upper limited by the maximum duty-cycle at a certain switching frequency.

[0054] Indeed, in order to obtain for example a duty-cycle of 90% at a switching frequency *of 200KHz*, the introduced delay should not be larger than 500ns, that is to say not greater than *Toff=(i-d)/fsw*.

[0055] Beyond this limit, the system would start to skip cycles, reproducing "too high" duty-cycle situation.

[0056] Thence, it may be useful to express the bandwidth increment as a function of the maximum allowed duty-cycle.

[0057] This relation is shown in Fig. 11.

[0058] With reference to the characteristics of Fig. 11, for example, for a delay *Td=250ns* at a switching frequency *fsw=200KHz*, the duty-cycle may range between 5% and 95% without skipping phenomena and with a bandwidth improvement factor of 1.5 referred to an amplifier made according to the prior art.

EXAMPLE OF AN EMBODIMENT

[0059] In practice, it is requested to realize a circuit that reproduces at an output a delayed replica of the PWM input signal.

[0060] Given that the delay *Td* to be introduced may be larger than the minimum time *Ton* (or *Toff*) of a phase of the PWM input signal, it is necessary to use two independent voltage ramps, respectively starting with the rising edge and with the falling edge of the digital input signal.

[0061] Fig. 12 shows a possible circuit diagram of the delay block that is introduced in the direct signal path of the PWM signal in an amplifier realized according to the present invention.

[0062] By referring to the scheme of Fig. 12, on the nodes *A* and *A'* there exist respectively the ramp starting with the rising edge of the input signal and the ramp starting with the falling edge of the input signal.

[0063] The slope of the voltage ramps is given by *-I/C*, where *I* is the discharge current of the capacitor *C*.

[0064] In order to better comprehend the functioning of the circuit, reference may be made to the waveforms of Fig. 13, which illustrate a whole switching period with an input signal with a duty-cycle of 50%.

[0065] When the input signal goes high, the *FF1* flip-flop is set and the capacitor *C* is discharged at a constant current *I*.

[0066] The voltage on the node A starts to decrease with a constant slope *I/C*.

[0067] When the voltage on the node *A* reaches the threshold *Vth* of the inverter, the voltage on the node *B* switches high and the FF_0 input flip-flop is set.

[0068] By way of simplicity, the inverters are symmetrical (that is *Vth=Vs/2*, being *Vs* the supply voltage), therefore the delay is given by:

$$Td = \frac{VsC}{2I}$$

[0069] Under these conditions, with the node *B* in a logic high state, the reset of the flip-flop *FF1* takes place when the input signal goes low. The reset of *FF1* determines the reset of the voltage ramp (the node *A* switching to a high logic state).

[0070] Similarly, it may be readily comprehended also the functioning of the lower branch of the circuit, starting from a falling edge of the input signal.

[0071] Fig. 14 illustrates a condition when the duration of the high input phases *Ton* is shorter than the delay *Td*. It may be observed that in this case, the reset of the *FF1* flip-flop follows directly the rising edge of the voltage on the node B. Therefore the duration of the set pulse of the output flip-flop FF_0 is determined solely by the delay of the flip-flop *FF1* and of the pair of inverters.

Claims

1. A class-D amplifier comprising an input integrating stage *(Op-Amp, R1, C)*, a modulating stage (PWM) of the integrated input signal output by said integrating stage, using as a carrier an alternate waveform (*Vtr*) of a frequency (*fsw*), sufficiently higher than the frequency band of the analog input signal, outputting a digital signal switching between a positive voltage (*+Vcc*) and a negative voltage (*-Vcc*), and whose average value (*Vo*) represents an amplified replica of the input analog signal, an output power stage (BUFFER), producing an output digital signal

(*Vout*), a feedback line constituted by a resistor (*R2*) connected between the output of said output power stage (BUFFER) and an input node of an operational amplifier (*Op-Amp*) constituting said integrating stage, and a low pass filter reconstructing an output analog signal (*Vo*), characterized in that it further comprises .

a delay stage (DELAY *Td*) functionally coupled in the direct path of propagation of said digital signal from the output of said (PWM) stage to an input of said output power stage (BUFFER), delaying said digital signal by a delay (*Td*) whose value is defined in function of a desired broadening of the. bandwidth and in consideration of the corresponding restriction of the range of variation of the duty-cycle of the output digital signal.

2. The amplifier according to claim 1 characterized in that said delay stage (DELAY *Td*) is constituted by a circuit defining two propagation paths of the digital input signal toward respective set and reset inputs of a bistable output circuit (FF_0),

a first path comprising a first bistable circuit (*FF1*) set by the input digital signal, the output Q of which drives a first inverter (*INV1*) charging a capacitor (*C*) discharged at a constant current (*I*), the charge ramp of said capacitor driving a second inverter (*INV2*) whose output is coupled to a set input of said bistable output circuit (FF_0) and to a first input of a logic AND gate receiving on a second input said digital input signal, inverted by a third inverter (*INV3*), the output of said AND gate being coupled to a reset input of said first bistable circuit (*FF1*);

a second path comprising a second bistable circuit (*FF2*) set by the inverted input digital signal, output by said third inverter (*INV3*), the output (*Q*) of said second bistable circuit (*FF2*) driving a fourth inverter (*INV4*) charging a capacitor (*C*) discharged in a constant current (*I*), the charge ramp of said capacitor driving a fifth inverter (*INV5*) whose output is coupled to the reset input of said bistable output circuit (FF_0) and to a first input of a logic AND gate receiving on a second input said input digital signal, the output of said AND gate being coupled to the reset input of said second bistable circuit (*FF2*).

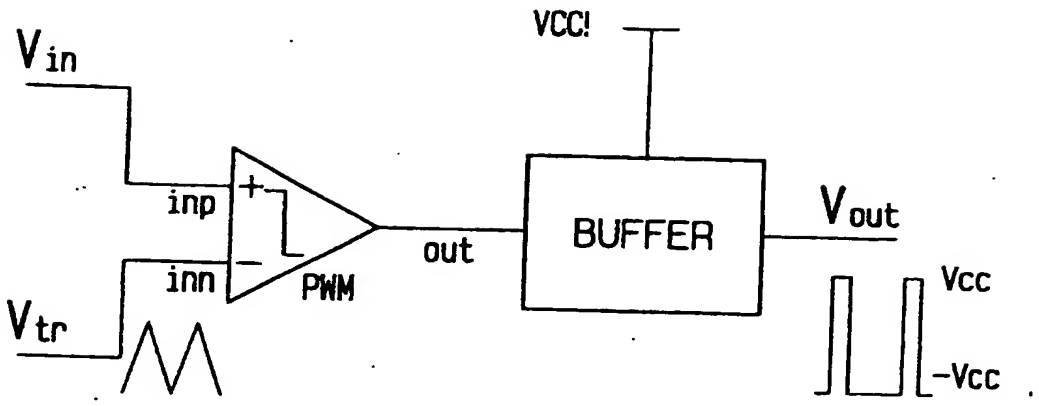
Vin
VCC!
inp
inn
PWM
out
BUFFER
Vout
Vtr
Vcc
-Vcc

FIG.1

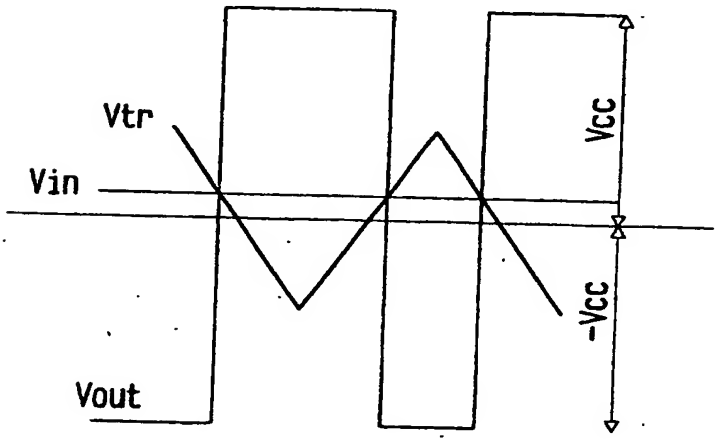
Vtr
Vin
Vout
Vcc
-Vcc

FIG.2

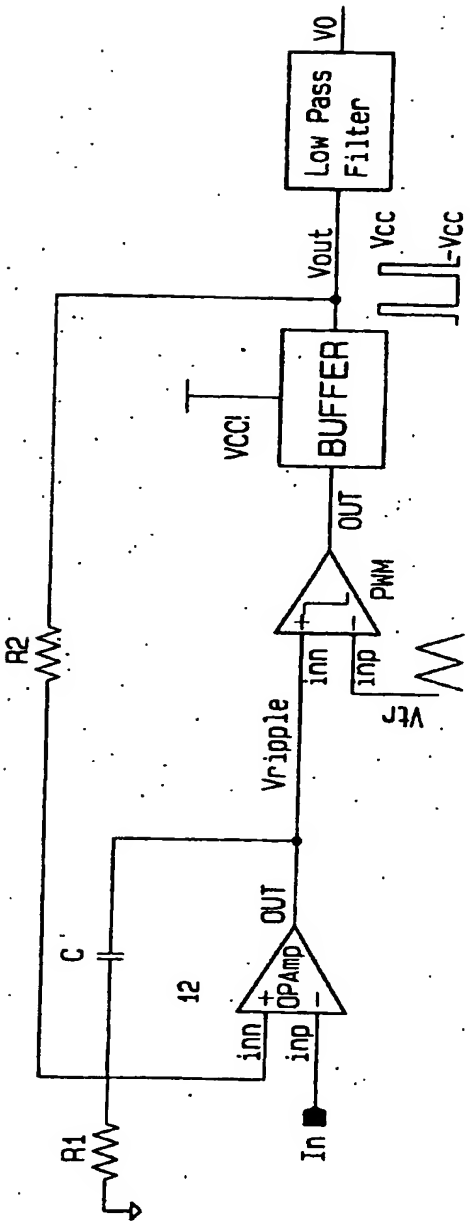
VO
Low Pass Filter
Vout
Vcc
-Vcc
VCC!
BUFFER
OUT
PWM
inn
inp
Vtr
Vripple
R2
C
12
OUT
OPAmp
inn
inp
R1
In

FIG.3

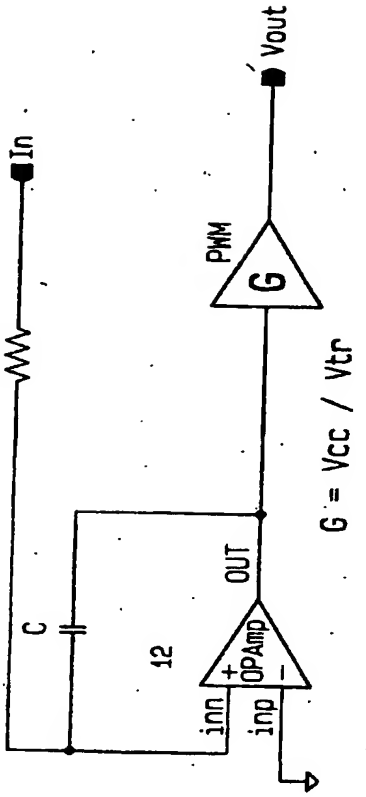
In
R2
C
12
OUT
OPAmp
inn
inp
PWM
G
Vout
G = Vcc / Vtr

FIG.4

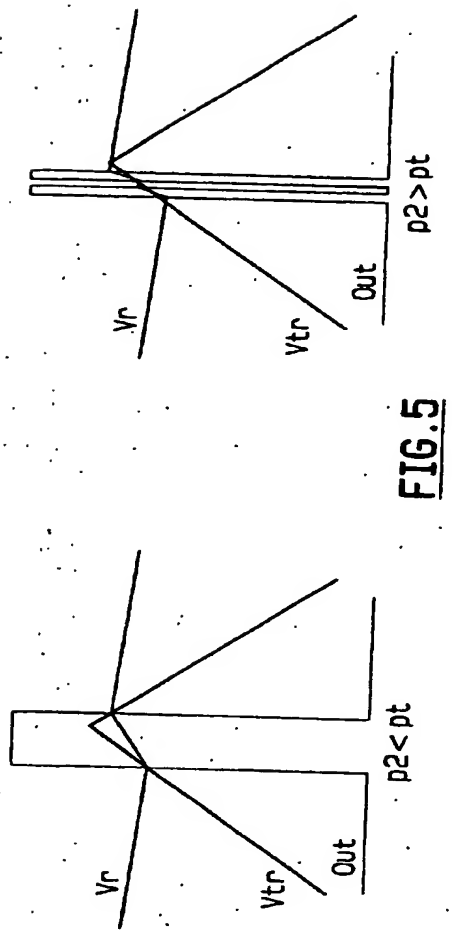
p2>pt
Out
Vtr
Vr
p2<pt
Out
Vtr
Vr

FIG.5

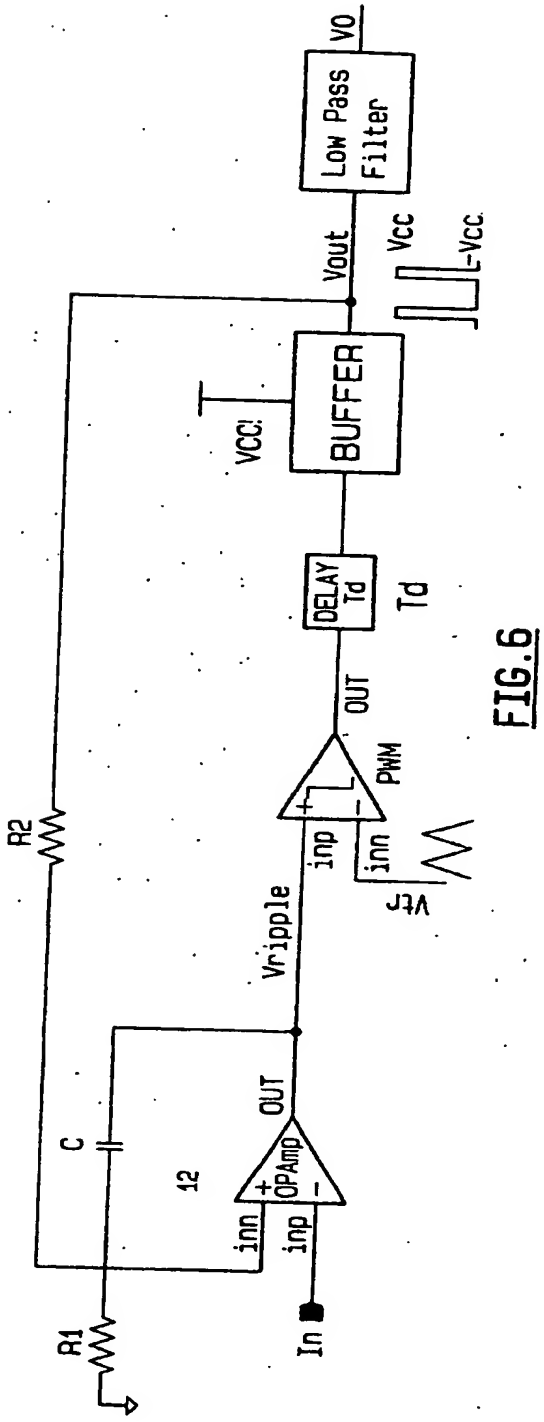
VO
Low Pass Filter
Vout
Vcc
-Vcc
VCC
BUFFER
DELAY Td
Td
OUT
PWM
inp
inn
Vtr
R2
Vripple
C
12
OUT
OPAmp
inn
inp
R1
In

FIG.6

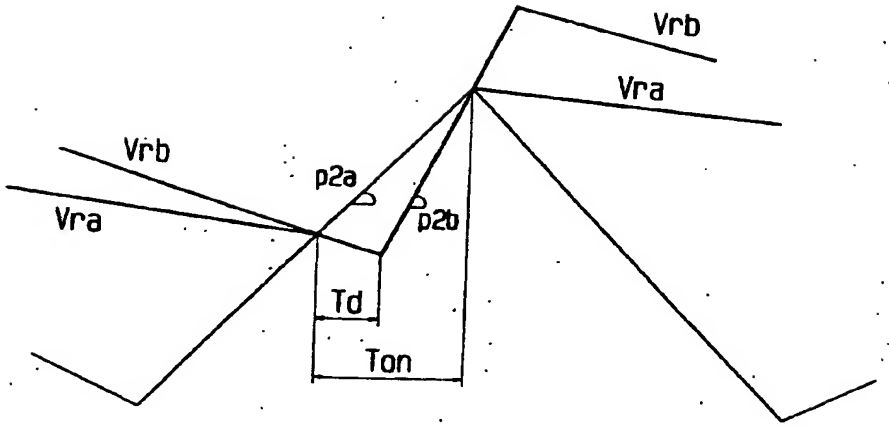
Vrb
Vra
Vrb
Vra
p2a
p2b
Td
Ton

FIG.7

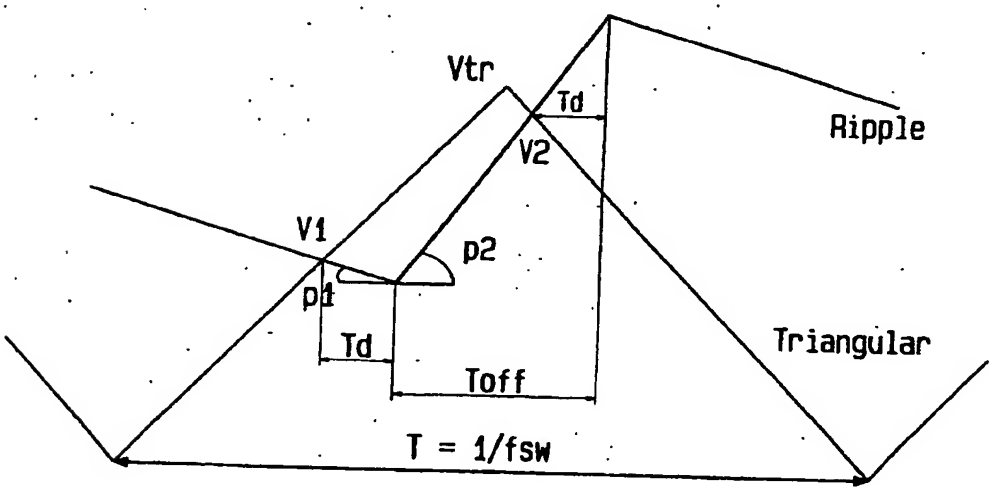
Vtr
Td
Ripple
V2
V1
p2
p1
Td
Triangular
Toff
T = 1/fsw

FIG.8

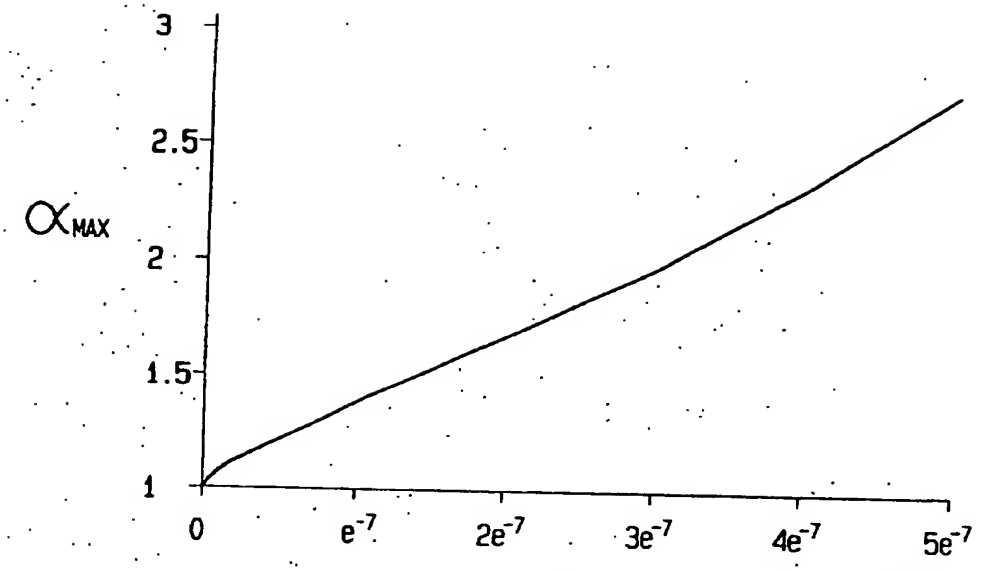
3
2.5
α_{MAX}
2
1.5
1
0
e^{-7}
$2e^{-7}$
$3e^{-7}$
$4e^{-7}$
$5e^{-7}$
Td (s)

FIG.9

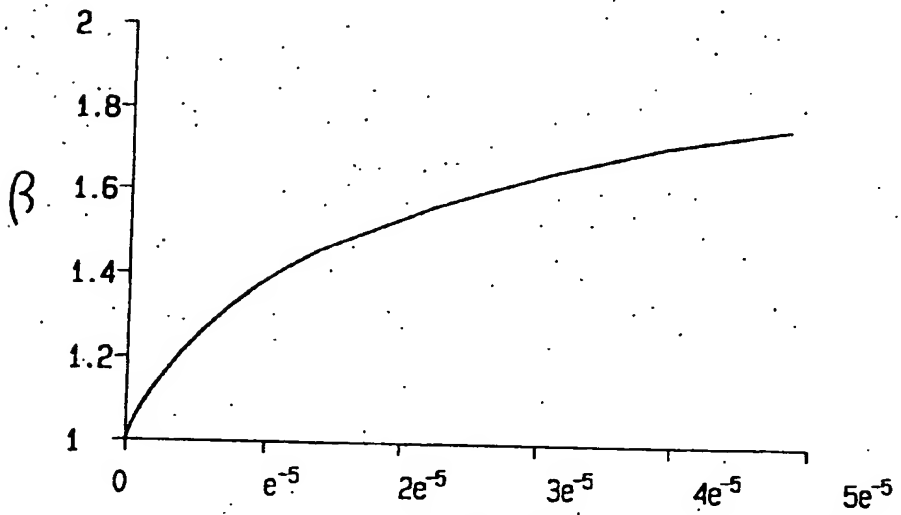
2
1.8
β
1.6
1.4
1.2
1
0
e^{-5}
$2e^{-5}$
$3e^{-5}$
$4e^{-5}$
$5e^{-5}$
Td (s)

FIG.10

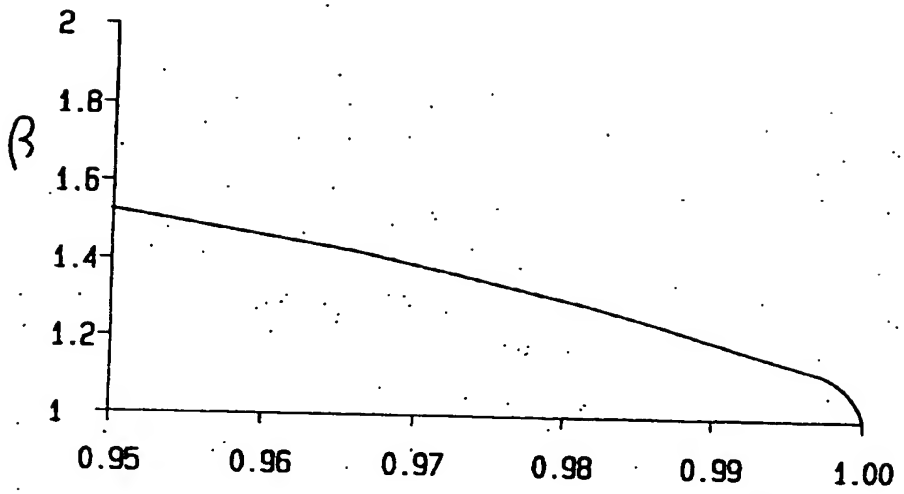
2
1.8
β
1.6
1.4
1.2
1
0.95
0.96
0.97
0.98
0.99
1.00
Dskip

FIG.11

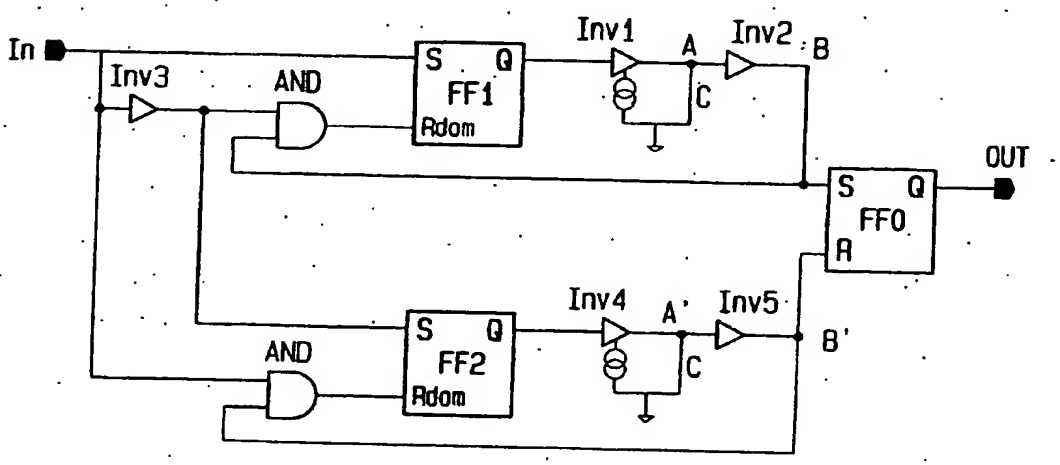
In
Inv3
AND
S Q
FF1
Rdom
Inv1
A
Inv2
B
C
OUT
S Q
FFO
R
Inv4
A'
Inv5
B'
AND
S Q
FF2
Rdom
C

FIG.12

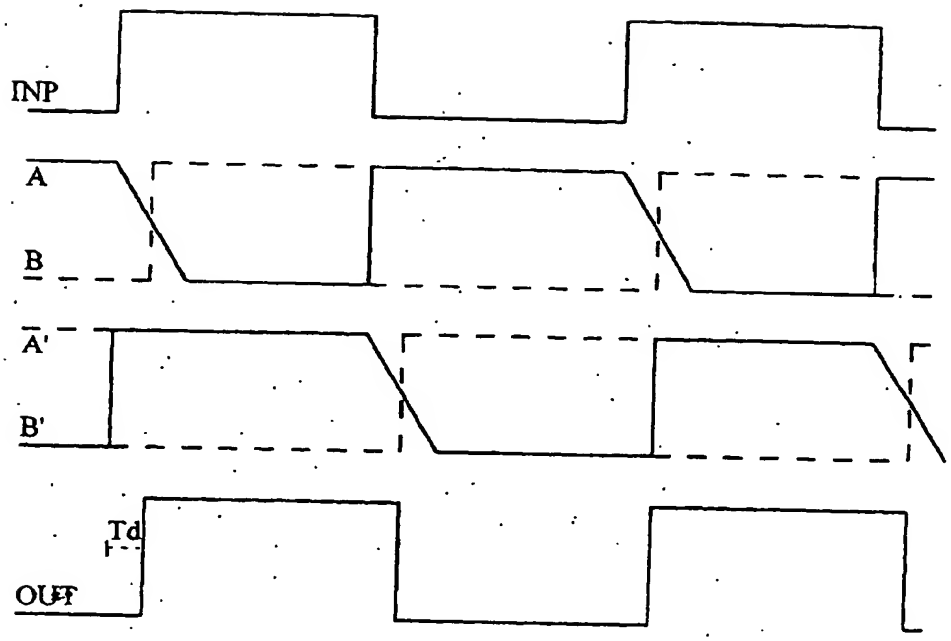

FIG. 13

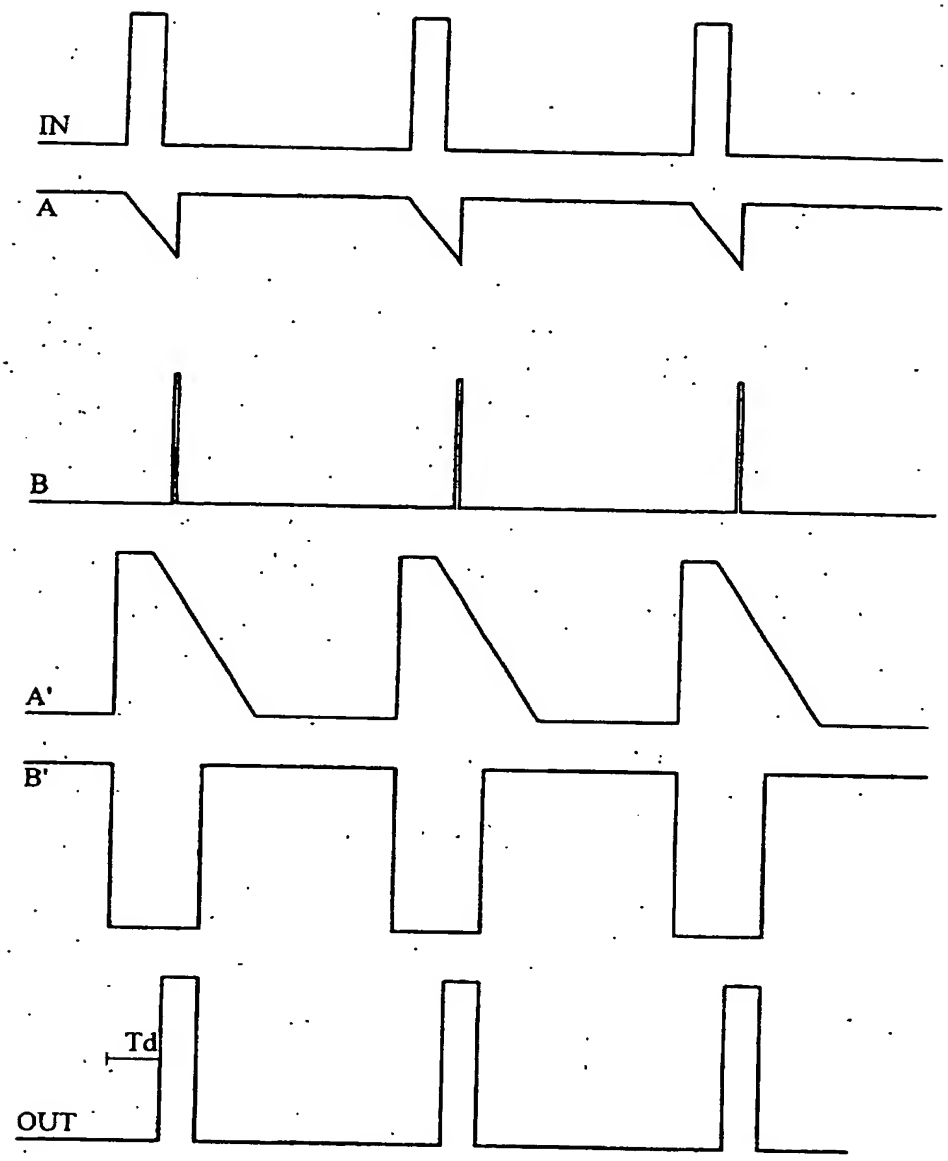

FIG. 14

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 4 649 565 A (KAIZER ADRIANUS J M ET AL) 10 March 1987 (1987-03-10) * column 9, line 22 - column 11, line 23; figure 7 *	1	H03F3/217
A	US 4 458 208 A (ABE MIKI) 3 July 1984 (1984-07-03) * column 3, line 21 - column 5, line 55; figures 3,4 *	2	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 September 1999	Tyberghien, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0247

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

30-09-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4649565 A	10-03-1987	NL 8203428 A	02-04-1984
		BR 8304704 A	10-04-1984
		DE 3329194 A	08-03-1984
		FR 2532806 A	09-03-1984
		GB 2126456 A,B	21-03-1984
		JP 1839042 C	25-04-1994
		JP 5052720 B	06-08-1993
		JP 59061209 A	07-04-1984
US 4458208 A	03-07-1984	JP 57170606 A	20-10-1982
		AU 550765 B	10-04-1986
		AU 8237382 A	14-10-1982
		CA 1173524 A	28-08-1984
		DE 3213269 A	04-11-1982
		FR 2503961 A	15-10-1982
		GB 2096850 A,B	20-10-1982
		NL 8201546 A	01-11-1982

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82